METHOD FOR MAKING AN ULTRA THIN FDSOI DEVICE
WITH IMPROVED SHORT-CHANNEL PERFORMANCE
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Cross-Reference to Related Application

This application is related to US Provisional Application No. 60/260,484, filed on January 9, 2001.

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Field of the Invention

This invention relates to semiconductor device manufacturing methods, and in particular to methods for forming ultra-thin Silicon-On-Insulator (SOI) device structures.

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Background of the Invention

As integrated circuit dimensions decrease and circuit speed increases, new transistor structures have been developed in order to yield good performance at the smaller dimensions. In particular, Silicon-On-Insulator (SOI) devices are known and are generally undoped or very lightly doped silicon on a low K dielectric. SOI devices are characterized by having the active device region insulated from the bulk substrate, generally by a buried oxide layer. The active device region is thereby said to be floating. SOI devices have been developed which consume less power than do bulk CMOS devices, and which operate at higher speeds than do bulk CMOS devices. Figure 1 shows a prior art SOI device, including bulk substrate 2, buried oxide layer 4, SOI silicon layer 6, field oxide regions 7, gate dielectric layer 8, conducting gate 10, gate sidewall spacers 11, doped source and drain regions 12, and channel region 14. Source and drain regions may overlap the

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gate region, or gate sidewall spacer technology may be used to provide separation, or underlap, between the gate and the source-drain regions.

5   For SOI devices having channel lengths below about 50 nm, in particular Fully Depleted Silicon On Insulator (FDSOI) devices, it is very difficult to achieve good short-channel control, i.e., to effectively shut off the transistors in the off state, without significantly thinning down the thickness of the buried layer and the thickness of the SOI silicon layer, which is difficult to reliably achieve with available processes. For a device with SOI silicon thickness of less than 20 nm, an underlap of the source/drain regions with the gate is needed in order to be able to

10   turn off the device. Accordingly, the details of the gate sidewall spacer technology used in the fabrication of such devices are critical to their performance. By way of example, it is known that if doped polysilicon spacers are used in place of nitride spacers (termed a "straddled gate device"), the device DC characteristics improve significantly. The polysilicon spacer which is also doped during source/drain

15   implant serves as a side gate with a lower work function. It behaves like a longer gate when there is no bias applied on the gate (i.e., in the Ioff condition). The polysilicon side gate causes the surface beneath it to invert at much lower applied voltage than the voltage necessary to invert the main channel region, due to the lower work function of the polysilicon. This causes the device to behave like a

20   very short channel device during Ion conditions. The result is a much improved Ion and Ioff. However, when single layer polysilicon gate sidewall spacers are used, the source/drain extension regions reach under the poly spacers and cause an increased overlap capacitance which slows down the AC device performance.

The formation of multiple sidewall spacers, including an inner polysilicon spacer and an outer oxide or nitride spacer, over a metal gate with CD's less than 50 nm, has not to the best knowledge of the inventors been achieved in the prior FDSOI art, but would achieve the desired DC and AC characteristics.

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Brief Summary of the Invention

It is therefore an object of this invention to provide a method for forming a Fully Depleted Silicon-On-Insulator device structure with a thin SOI silicon layer and a channel length less than 50 nm, which maintains excellent Ioff DC

10 characteristics without degrading device AC speed and characteristics.

It is a further object of this invention to provide a method for forming a Fully Depleted Silicon-On-Insulator device structure with a thin SOI silicon layer and a channel length less than 50 nm which utilizes a tapered polysilicon etch to form inner polysilicon spacers and which utilizes deposited metal within the etched

15 region.

Brief Description of the Figures

Fig. 1 shows a prior art SOI device structure.

Fig. 2 shows a process flow for the inventive process.

20 Fig. 3a illustrates an intermediate structure following formation of a MOS SOI structure after step 42.

Fig. 3b illustrates an intermediate active gate region structure resulting after the polysilicon spacer etch after step 50.

Fig. 3c illustrates the final active gate region structure following deposition

25 and polishing of metal into the etched region after step 58.

Fig. 4 illustrates an embodiment of a completed FDSOI device active region made by our process.

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Detailed Description of the Invention

Figure 2 shows a process flow for the inventive process. Intermediate structures resulting at stages of the process are illustrated in Fig's 3a – 3c.

Steps 16 – 42 provide the formation of a conventional MOS SOI structure using techniques known in the art.

In step 16, a bulk substrate 60 is provided having a buried oxide layer 62 thereon, usually undoped SiO_2 with thickness of approximately 50 - 60 nm, and a thin undoped SOI silicon layer 64 of approximately 5 – 20 nm atop the buried oxide layer 62.

In step 18, temporary gate dielectric 66 is grown and/or deposited using standard methods atop the SOI silicon layer 64, comprising silicon dioxide alone or in combination with other dielectric such as silicon nitride, with a total equivalent oxide thickness of 0.6 – 2.0 nm.

In step 20, approximately 75 – 100 nm of polysilicon 65 is deposited atop the temporary gate dielectric 66, then 20 – 36 nm of SiON 67 is deposited atop the polysilicon.

In step 22, the polysilicon/SiON layer is patterned and etched using known lithographic and etching techniques to provide a gate poly feature 68 with length of 40 – 75 nm.

In step 24, implantation of extension implanted regions 70 is performed. For p-channel devices, extension implantation may be 1-2e14/cm^2 BF2 at 10 –15 keV. For n-channel devices, extension implantation may be 0.5 – 2 e14/cm^2 As at 3-5 keV.

In step 26, RTA anneal for 5-10 seconds at 900 – 950C is performed.

In step 28, 70 – 90 nm silicon nitride is deposited by standard deposition techniques.

In step 30, the nitride of step 28 is anisotropically etched using standard dielectric etch processes, leaving nitride spacers 72 on the polysilicon sidewalls 74. Exposed portions of the temporary gate dielectric 66 are removed during the nitride etch.

5   In step 32, implantation of source/drain regions 76 is performed. For n-channel devices, source/drain implantation may be $2\text{-}3e15/cm^2$ P at 7-13 keV. For p-channel devices, source/drain implantation may be $2\text{-}3e15/cm^2$ B at 1.5 – 3 keV. The gate poly 68 is also doped during the source/drain implantation step.

In step 34, RTA anneal for 5-10 seconds at 950 – 1025 C is performed.

10   In step 36, 20 –25 nm silicon 78 is grown by a selective epi process.

In step 38, 10-12 nm cobalt is deposited.

In step 40, the wafer is annealed a 650 – 800 C for 15 – 60 seconds to convert the selective epi layer to cobalt silicide 80. The unreacted cobalt is removed by a standard wet strip process in step 41.

15   In step 42, 150 – 200 nm TEOS 82 is deposited and polished back to the top of the SiON layer 67, using standard deposition and CMP processes. Figure 3a illustrates the intermediate structure resulting following process step 42.

Steps 44- 50 are an embodiment of an inventive process flow which

20   provides for the formation of tapered doped poly spacers inside the gate opening.

In step 44, the wafer is installed in an oxide RIE machine such as the Applied Materials MxP+, and standard selective RIE etch is performed to remove the SiON layer 67. The high selectivity of the etch insures minimal loss of TEOS 82 or nitride 72, and acceptable loss of the polysilicon 65 (which is non-critical).

25   In step 46, the wafer is installed in a poly RIE machine such as the Applied Materials DPS system, and RIE poly etch is performed using a mixture of Cl_2 and HBr with He and oxygen, which has a very high selectivity of poly etch rate to

oxide etch rate (on the order of 40 – 50:1), etching through the gate poly layer 65 and stopping on the temporary gate dielectric 66. The high selectivity allows for approximately 100% overetch. This etching step includes a) adjusting the Cl_2/HBr ratio and b) adjusting the temperature of the wafer chuck to provide the desired

5   amount of taper of the etch walls 84. Temperatures can range between 30 and 70 C, and Cl_2/HBr ratio can range between 0.5 and 1.5. The amount of taper is chosen to leave a base of approximately 10 – 20 nm of poly at the bottom 86 of each poly spacer 88. This corresponds to a sidewall angle of approximately 75 – 85 degrees from horizontal for poly thickness of 75 nm, assuming the poly spacer thickness of

10   zero at the top 90 of the spacers 88. The aforementioned etch chemistry, while known in the art, is not generally applied to the etching of polysilicon lines, due to the tapered sidewalls which result. However, according to our invention, taper of 75-85 degrees is desirable and therefore the selected etch chemistry is suitable.

In step 48, standard wet etching is performed to remove the remaining

15   exposed temporary gate dielectric.

In step 50, wet etch in a mixture of NH_4OH and H_2O_2 is performed to remove approximately 30 Angstroms of silicon below the etched region 92, to provide a thinner channel which yields better short-channel control. Figure 3b illustrates the intermediate structure of the active gate region, resulting following

20   process steps 44-50.

Steps 52- 58 are further embodiments of the inventive process flow which provides for the formation of final gate dielectric and metal inside the gate opening.

25   In step 52, final gate dielectric 94, comprising by way of example 6 Angstroms silicon dioxide followed by 10 Angstroms silicon nitride, is deposited at low temperature, rather than grown by thermal oxidation. This is necessitated

by the inability of the silicide 80 to withstand the high temperatures utilized in an oxidation furnace. Low temperature dielectric deposition yielding suitable quality gate dielectric has been successfully performed in the Remote Plasma Processing Tool from Applied Materials, at a temperature of approximately 300 C.

5   In step 54, the wafer is annealed at the highest acceptable temperature, generally about 800C for approximately 1 − 3 minutes to produce a high quality dielectric 94 and dielectric-silicon interface 96. The presence of the dielectric 94 on poly spacer sidewalls 84 prevents intermixing of the metal electrode and the poly spacers, thereby providing a well-defined gate work function.

10   In step 56, metal 98 is deposited into the etched region 100, atop the gate dielectric 94. CVD deposition of mid-gap metals such as TiN or W may be utilized if a single metal deposition is used for both n- and p-channel devices. Alternatively, the metal deposition process and subsequent polish step may be repeated separately for n- and p-channel devices while masking the other device 15 types, if the metal is to be separately optimized for n- and p-channel devices. This alternative increases process complexity, but provides for improved device characteristics. In step 58, CMP is performed to polish away the residual metal 98 from the top of the TEOS layer 82. In step 60, a short wet etch removes a small amount of gate dielectric 94 at the top of the poly spacer sidewalls 84, extending 20 less than halfway down the sidewalls, to assure that subsequent conducting contacts reach the metal electrode and both poly sidewall spacers when applying gate bias.

Figure 3c illustrates the final structure of the active gate region. Metal gate 98 is separated from silicon 64 by gate dielectric 94. Two sets of gate sidewall 25 spacers include tapered doped poly spacers 88 and dielectric spacers 72. Channel length 102 is determined by the width of metal 98 at its bottom.

Our inventive method, including formation of an MOS structure having a
doped polysilicon gate, then etching the poly to leave tapered poly spacers and
depositing gate dielectric and metal into the etched region, provides channel length
102 as small as 20-35 nm according to the poly spacer dimensions outlined above.

5 CVD metal deposition is known to be able to fill such a small gap, and the tapered
sidewalls increase the effectiveness of the metal fill. The gate work function is
determined by the bottom 25 Angstroms of metal, so the deposited metal must be
of high quality for at least that thickness. In contrast, using state of the art
patterning and etching techniques for metal lines, critical dimensions and channel

10 lengths are typically 90 nm or greater. Additionally, the metal configuration using
our process, whereby the metal is wider at the top, lowers gate resistance while
maintaining short channel length.

Standard contact and metallization processes follow the inventive formation
of the gate region of the device. Figure 4 illustrates a completed FDSOI device

15 active region made by our process. Metal gate 98 which is wider at the top defines
channel length 102 less than 50 nm. Double sidewall spacers include tapered
doped poly spacers 88 and nitride spacers 72. Deposited gate dielectric 94
separates metal gate 98 from SOI silicon 64.

20 We have provided an inventive method for forming a Fully Depleted
Silicon-On-Insulator device structure with a thin SOI silicon layer and a channel
length less than 50 nm, having inner polysilicon spacers and outer dielectric
spacers, which maintains excellent I_{off} DC characteristics without degrading device
AC speed and characteristics.

25 Device simulations using the Medici simulation program by Avanti show
that the DC Ioff characteristics are comparable to those achieved with only
polysilicon spacers; the Ion characteristics are within 2-3% of those achieved with

only polysilicon spacers. The AC characteristics, specifically the inverter ring oscillator stage delay, are significantly improved compared to a device having only polysilicon spacers. The AC characteristics are within 10% of the values achieved with devices having only silicon nitride spacers, but with much improved short

5   channel control.

It is not intended that the invention be restricted to the exact embodiments described herein. For example, the processing details, including temperatures, times, implant energies and doses, and exact metal and dielectric materials used,

10   may be altered without departing from the inventive concept. Alternative metals for n-channel devices include: PVD or CVD Al, electroplated Co or its alloys (CoWP, CoWB), and Cr and its alloys. Alternative metals for p-channel devices include: CVD or electroplated Ni, electroplated Pd or its alloys (SnPd), or Atomic Layer Deposited RuO_2. Alternative metals for mid-gap electrodes include:

15   electroplated Cu, Ag, and Ir and their alloys. The scope of the invention should be construed in view of the claims.

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